Partial English Translation of

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JAPANESE PATENT APPLICATION

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[0021] to [0033]

[0021]

[Embodiments] The present invention will be described in detail based on embodiments.

[0022] (First Embodiment) Next, a first embodiment of the present invention will be described with reference to Figure 1. Although the semiconductor substrate used in the present invention may be a silicon monocrystal substrate or an SOI substrate, the below explanations refer to a case where a silicon substrate is used.

[0023] Firstly, for element isolation, a field oxide film 2 is formed to 3500 Å on a silicon substrate 1 by a selective oxidation method, as shown in Figure 1(a). Further, a gate oxide layer having a thickness of 70 Å and a polysilicon layer having a thickness of 2000 Å are sequentially stacked in the thus formed element formation region and are processed by photolithography and etching, so that a gate oxide film 3 and a polysilicon layer 4 to be as a part of a gate electrode 5 are formed. Thereafter, using the polysilicon layer 4 as a mask, P^+ ions and As^+ ions are implanted, with self-aligned, at accelerating energies of 30 keV and 40 keV in dose amounts of 2×10^{13} cm^{-2} and 5×10^{13} cm^{-2}, respectively, so that a lightly doped diffusion layer (not shown in the drawing) is formed in source/drain region 7.

[0024] Then, a HTO film (High Temperature Oxide: a high temperature CVD oxide film) is entirely formed to 1400 Å and is subjected to anisotropic etching, so that a sidewall spacer 6 is formed on the both sides

of the polysilicon film 4. Thereafter, the source/drain region 7 is formed, and impurities are introduced into the polysilicon film 4 in a manner that impurities are heavily implanted into a region to serve as the source/drain region and the polysilicon film 4. Wherein, $^{49}BF^{2+}$ ions and $75As^{+}$ ions are implanted at accelerating energies of 40 keV and 50 keV in dose amounts of 2×10^{15} and 3×10^{15} cm^{-2}, respectively. After the ion implantation, a furnace anneal thermal treatment is performed at a temperature of 800 to 900 ℃ for 5 to 60 minutes for activation of the thus implanted ions and recovery in crystals of the silicon substrate 1.

[0025] Next, a high melting point metal film 9 is entirely formed by a sputtering method, a vacuum deposition method and a selective CVD method or the like. The high melting point metal film 9 is formed of, for example, W, Ta, Ti, Co, Ni and Pt, and preferably has a film thickness of approximately 150 Å to 700 Å. When the film thickness thereof is less than 150 Å, the thickness of a silicide film 10 on the source/drain region 7 is small, whereby the sheet resistance thereof is high. On the other hand, when the film thickness thereof is over 700 Å, the thickness of the silicide film 10 on the source/drain region 7 is large and hence, is close to the source/drain region, whereby the leak current thereof is increased.

[0026] By performing a thermal treatment subsequent thereto, the high melting metal film 9 solid-reacts with the source/drain region 7 in contact with the high melting metal film 9 and silicon in the polysilicon film 4 in the upper part of the gate electrode part 5, whereby the silicide film 10 is formed. A high melting point metal film 13 in contact with an atmospheric gas at the thermal treatment reacts with the atmospheric gas, resulting in that a reactant is formed on the surface thereof. The purpose of this thermal treatment is to cause a reaction of the high melting point metal film 13 with the source/drain region and silicon in the surface portion of the polysilicon film 4 of the gate electrode part 5, and a lamp anneal method (Rapid Thermal Anneal method), an electric furnace anneal

method and the like can be used.

[0027] Herein, the anneal is preferably performed in an atmosphere of an inert gas such as nitrogen. Further, the thermal treatment is preferably performed at a temperature of approximately 600 ℃ to 750 ℃ for approximately 20 to 60 seconds. In so doing, a part of the high melting point metal film 13 formed directly on the silicon substrate 1 reacts with silicon, leading to the formation of the silicide film 10. The thickness of the silicide film formed by the thermal treatment is approximately 100 to 1000 Å and the thickness of the reactant formed on the surface of the high melting point metal film 13 is approximately 50 to 500 Å. In the present embodiment, a Ti film 13 having a thickness of approximately 200 Å is entirely formed on the silicon substrate 1, and the silicide film 10 is formed in a manner that RTA is performed in a nitrogen gas atmosphere for 40 seconds at a temperature of 700 ℃. In this thermal treatment, a titanium silicide ($TiSi_2$) film 10 is formed in a region where Ti is in contact with Si and titanium nitride (TiN) is formed in the surface portion of the Ti film 13 in contact with the nitrogen gas. Next, as shown in Figure 1(b), after the silicide film 10 is formed in the upper part of the gate electrode part 5, a reactant of the nitrogen gas and the non-reacting Ti film 13 is removed. The method of removing the reactant is not particularly limited. For example, according to the first method, the reactant is removed by performing a reactive ion etching after photolithography. When the reactant is TiN, the reactive ion etching can be performed under the conditions that the flow rates of BC13 and C12 as etching gases are respectively 20 to 150 sccm and 50 to 200 sccm, the pressure is approximately 10 to 20 mTorr and an etching power is approximately 100 to 500 W. Under the above conditions, the selection ratio between the oxide film and TiN is approximately 7 to 15. If this method is used, the gate electrode part 5 is not severely etched since the selectivity is secured between TiN formed in the upper part of the gate electrode part 5 and the

silicide film 10 forming the gate electrode part 5 and between the polycrystal silicon film 4 and the sidewall spacer 6. Moreover, a margin can be provided since displacement of alignment at the photolithography can be allowed for the width of the sidewall spacer 6.

[0028] As the second method, the well known chemodynamic polishing method can be used. In the chemodynamic polishing method, the Ti film 13, in the surface portion of which TiN is formed, is polished and removed by rotating a wafer approximately 40 to 50 rpm while applying pressure at approximately 200 to 400 g/cm^2. Herein, gentle polishing is required since TiN is very thin.

[0029] According to the third method, after photography is performed in the same manner as in the first method, TiN is etched and removed, using a fluid. As the fluid for dissolving TiN, it is possible to use a solution mixture obtained by mixing a hydrogen peroxide solution, an ammonia solution and water in a ratio of 1 : 1 : 3 to 8 at a temperature of 50 to 80 ℃. When this method is used, there can be also secured the selectivity between TiN formed in the upper part of the gate electrode part 5 and the silicide film 10 and between the polysilicon film 4 and the sidewall spacer 6. It is to be noted that the most preferable method among the aforementioned three methods for removing the reactant on the gate electrode is the first method using the reactive ion etching. The reason for this is that, since the reactive ion etching is anisotropic, it is possible to remove only a part of which TiN is necessary to be removed.

[0030] Then, as shown in Figure (c), the silicidation reaction of the polysilicon film 4 of the gate electrode part 5 is promoted in a manner that the high melting point meta film 19 is deposited and the thermal treatment is performed. However, no silicidation reaction is promoted in the source/drain region 7 where no TiN is removed. As a result, it becomes possible to increase the thickness of the silicide film 14 of the gate electrode part 5 without increasing the thickness of the silicide film 10 on

the source/drain region 7. Note that, as the high melting point metal film 19 formed on the gate electrode part 5, it is not necessary to employ the same type of metal as the high melting point metal used for the silicide film 10 formation. Further, the thickness of the high melting point metal to be deposited can be arbitrarily determined according to the thickness of a desired silicide film formed on the gate electrode. Moreover, ion implantation for promoting the silicidation reaction may be performed before or after depositing the high melting point metal.

[0031] Herein, the energy and amount of the ion implantation can be arbitrarily determined. For example, when there is employed such a low energy level that the ion implantation can be performed only to the silicide film 10 of the gate electrode part 5 where TiN is selectively removed, the silicide film 10 on the source/drain region 7 is protected by the Ti film 19, thereby receiving no influence of the ion implantation. Accordingly, it becomes possible to promote the silicidation reaction only in the polysilicon film 4 of the gate electrode part 5. On the other hand, when there is employed such a high energy level that the ion implantation can be performed to the silicide film 10 on the source/drain region 7, the silicide film 10 which has been formed once is made amorphous to promote a phase transition in the lower resistance layer, whereby the resistance can be made lower without involving no change in the thickness of the silicide film 10. Furthermore, it goes without saying that the silicidation reaction is promoted in the polysilicon film 4 of the gate electrode part 5 when the ion implantation is performed at a high energy level.

[0032] As a method for removing the reactant on the gate electrode, there can be used a method of performing photolithography or the like and then, removing the reactant by the reactive ion etching. Thereafter, the Ti film 19 having a thickness of approximately 500 Å is entirely formed, and lamp anneal (RTA) is performed at a temperature of 700 ℃ for 40 seconds under an atmosphere of a nitrogen gas, so that the silicide film 14

is formed only in the polysilicon film 4 of the gate electrode part 5. In this time, TiN remaining on the source/drain region 7 blocks the silicidation reaction, and accordingly, the thickness of the silicide film is not increased. More specifically, arbitrary selection can be made from, for exampl, Si, Sb, As, Ga, Ge in ions to be implanted 10 Kev to 50 KeV in the implantation energy and 5×10^{14} to 1×10^{16} cm^{-2} in an amount.

[0033] Next, as a method for removing at one time the non-reacting Ti film 13 and TiN as a reactant formed on the surface thereof, the Ti film 13 and the TiN are immersed in a mixture solution of a sulfuric acid solution and a hydrogen peroxide solution for 30 minutes and in a mixture solution of an ammonia solution and a hydrogen peroxide solution for 2 minutes. When this method is used, the Ti film and the TiN film on the source/drain region 7 and on the gate electrode part 5 can be simultaneously removed. Thereafter, the lamp anneal is performed at a temperature of 850 ℃ for 10 seconds under an atmosphere of a nitrogen gas for lowering the resistance of the silicide film 14. Next, as shown in Figure 1(d), after the interlayer insulating film 11 is formed, a contact hall 12 is formed in a predetermined position. In this way, a contact electrically connected to the source/drain region 7 of the each transistor is formed.